JEDEC PUBLICATION

FOUNDRY PROCESS QUALIFICATION GUIDELINES – BACKEND OF LINE

(Wafer Fabrication Manufacturing Sites)

JEP001-1A

(Revision of JEP001A, February 2014)

SEPTEMBER 2018

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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Published by
©JEDEC Solid State Technology Association 2018
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

PRICE: Contact JEDEC

Printed in the U.S.A.

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(Wafer Fabrication Manufacturing Sites)

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Foreword

The publication is divided into three parts, backend of line (JEP001-1A), transistor level (JEP001-2A), and product level testing (JEP001-3A). The document provides methodologies for the minimum set of measurements to qualify a new semiconductor wafer process. It is written with particular reference to a generic silicon based CMOS logic technology. While it may be applicable to other technologies (e.g., analog CMOS, bipolar, BICMOS, GaAs, etc.), some sections apply specifically to CMOS. No effort was made in the present document to cover all the qualification requirements for specific other technologies, e.g., Cu/Low K interconnects or ultra-thin gate oxide.

Any qualification requirements beyond the minimum set are to be developed for the specific performance expected of the technology. The minimum set of measurements and the requirements for the qualification based on those measurements are to be determined between the foundry and its customers on an individual basis The process technology owner (foundry) will be required to document the details of specific testing unique to the process being qualified.

The guideline documents common best practices in the semiconductor industry and updated in accordance to advancement in the semiconductor industry and JEDEC bylaws of periodic reviews.

Introduction

This publication, was originally published as JP-001 entitled 'Foundry Process Qualification Guidelines', it was co-sponsored by JEDEC and the FSA (Fabless Semiconductor Association). It originated at the FSA as a technology specific document, and has evolved into a generic set of qualification methodologies. The JEDEC sponsoring committee is JC-14 through its JC-14.2 subcommittee on wafer level reliability.

This document encompasses and references a number of other standards and procedures, some of which are in a state of constant revision and update. While a case might be made for producing a lean, concise guideline that does not spell out specific procedures or requirements, the proposition of spelling out the essence of a comprehensive set of methodologies in one place has a practical value that outweighs the case for simplicity.(comment : the requirements are only spelled out in a number of cases. Best to be consistent and let the existing JEDEC specs speak for themselves)

This publication is split into three parts: JEP001-1A, JEP001-2A, and JEP001-3A as described below. It is intended that each part references the appropriate test and requirement noting that some tests may be performed on the package level. This standard should be read alongside reliability requirements established between the supplier and customer.

The structure of the JEDEC JEP001 series as currently conceived is as follows:

Part 1 – Backend of line testing
Part 2 – Transistor-level testing
Part 3 – Product-level testing

Acronyms

The following acronyms have been used in this document:

WLR: wafer level reliability
EM: electromigration
SM: stress migration/voiding
IMD: inter/intra-metal dielectric
VRDB: voltage ramp dielectric breakdown
TDDB: time-dependent dielectric breakdown
QBD: Charge to breakdown
TVS: triangular voltage sweep

HTOL: high temperature operating life
EFR: early failure rate
FIT: Failures in time
THB: temperature-humidity bias
HAST: highly-accelerated stress test
ESD: electrostatic discharge
TQV: technology qualification vehicle
PCM: process control monitor
FA: failure analysis
TC: temperature cycling

FOUNDRY PROCESS QUALIFICATION GUIDELINES – BACKEND OF LINE (Wafer Fabrication Manufacturing Sites)

(From JEDEC Board Ballot JCB-17-31, formulated under the co-sponsorship of the JC-14.2 Subcommittee on Wafer Level Reliability.)

1 Scope

This document describes backend-level test and data methods for the qualification of semiconductor technologies. It does not give pass or fail values or recommend specific test equipment, test structures or test algorithms. Wherever possible, it references applicable JEDEC such as JESD47 or other widely accepted standards for requirements documentation.

There are two levels of qualification described. Level 1 is a pure process qualification intended to find reliability weaknesses. It primarily addresses technology wearout mechanisms through package or wafer level reliability tests on specially designed test structures.

Level 2 demonstrates the reliability of the process that corresponds to the reliability demands from projected or known applications. Level 2 testing can be implemented via the testing of a relevant functional technology qualification vehicle (TQV), including life test. The level 2 tests are described in Section 12. Other Reporting requirements (e.g., PCM data) are also included.

2 Quality system

It is the responsibility of the foundry to have the appropriate quality system in place with special emphasis on issues relating to equipment capability, maintenance and calibration, continuous improvement and process control. In particular, a functioning SPC methodology should be demonstrated for all key processes (see EIA/JEDEC EIA-557A). As a minimum the foundry will have ISO9001 certification. The ISO9001 audit results by a third party and subsequent corrective actions on deficiencies shall be made available to the customer upon request. For those supplying to automotive applications, the foundry may also have to demonstrate requirements from the IATF TS 16949 standard to meet the needs of these products

3 Responsibilities

3.1 Level 1 qualification

The foundry is responsible for the design and implementation of the level 1 test vehicle (i.e., TESTCHIP). For the special case of a foundry customer driving process development, development of the level 1 test vehicle may be shouldered in whole or in part by the customer. The foundry shall fabricate the qualification silicon, execute the described level 1 tests and create the qualification report. The tests and qualification report may be done by the foundry or third party test vendor. The qualification requirements may be reduced for a derivative process, where the parent process has already been fully qualified at the same location.

3.2 Level 2 qualification

In general, the foundry is responsible for the design and implementation of the Level 2 test vehicle (e.g., SRAM or pilot product). For the special case of a foundry customer driving process development, or where the customer requires TQV data before such a vehicle becomes available, development of the level 2 test vehicle may be shouldered in whole or in part by the customer. The foundry, customer or third party test vendor may execute the Level 2 (TQV) tests and requisite failure analysis. The foundry will be responsible for suggesting and implementing corrective action based on the failure analysis results. The qualification report shall adhere to the minimum reporting requirements and format described herein.

While it is expected that a particular foundry methodology may differ from the methods outlined in this document, the wafer foundry should demonstrate to the customer that it has satisfactorily addressed all issues of interest. The wafer foundry should therefore provide a documented procedure and supporting data that provide an assessment of potential failure and wearout mechanisms.

3.3 Reporting Requirements

Specific reporting requirements are included for the tests catalogued in this document. General reporting requirements include appropriate signoff, archiving and revision control, and the inclusion of supporting documents as appropriate.

The level 1 qualification report shall include: (1) qualification plan, (2) description of the test vehicle including relevant test structure features and dimensions, (3) summary of test methods used, (4) pass/fail criteria and (5) test results, analysis and model parameters as described in this document.

The level 2 qualification report shall include: (1) qualification plan, (2) description of the technology qualification vehicle (TQV), (3) test description & specification, (4) pass/fail criteria (5) test results & analysis including failure rates and (6) FA results.

4 Sample size

In general, data should come from 3 non-consecutive wafer lots, although the use of more lots is not precluded. A wafer lot is a group of wafers processed as a batch through the same or matched equipment in the same processing interval, using the same or matched conditions, materials, and methods. Typical sample sizes per lot are given in the individual test descriptions. Where applicable, confidence limits for each test population should be calculated. A conservative estimate of 40 die per wafer was made in determining sample size for tests that required the usage of all dies on the wafer.

5 Use of packages

Packages with a wire-bonded die that are capable of higher temperatures are generally used for testing of the technology qualification vehicle (TQV) or pilot product. A qualification report for the standard wire-bonding process should be included. Advanced packaging (e.g., BGA, flip-chip or chip-scale) may be substituted where applicable. This, in combination with TC and THB tests, will demonstrate the assembly capability of this wafer fab process.

Side brazed ceramic packages are generally required for process wear-out tests performed at package-level at Temperatures greater than 155 °C. Consequently, wafer level testing is recommended wherever possible.

All references to temperature in the following sections imply junction temperature unless otherwise specified.

6 Reference documents

6.1 Industry standard documents

The following reference documents contain provisions that, through reference in this text, constitute provisions of this document. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based in this publication are encouraged to investigate the possibility of applying the most recent editions of the reference documents indicated below. For undated references, the latest editions of the reference document referred to applies. Check the JEDEC website at http://www.jedec.org.

6.1.1 Reliability assessment methodology

JEDEC JEP70, *Quality and Reliability Standards and Publications.*

JEDEC JEP132, *Process Characterization Guidelines.*

JEDEC JEP143, *Solid State Reliability Assessment and Qualification Methodologies.*

JEDEC JEP122, *Failure Mechanisms and Models for Silicon Semiconductor Devices.*

JEDEC JESD91, *Method for Developing Acceleration Models for Electronic Component Failure Mechanisms.*

JEDEC JESD94 Application Specific Qualification Using Knowledge Based Test Methodology

JEDEC JESD659, *Failure-Mechanism-Driven Reliability Monitoring.*

JEDEC JEP131, *Process Failure Mode and Effects Analysis (FMEA).*

6.1.2 Electromigration, stress migration and IMD dielectric integrity

ASTM F1260M-96, *Standard Test Method for Estimating Electromigration Median Time-To-Failure and Sigma of Integrated Circuit Metallization.*

JEDEC JESD33, *Standard Method for Measuring and Using the Temperature Coefficient of Resistance to Determine the Temperature of a Metallization Line.*

JEDEC JESD37, *Standard Lognormal Analysis of Uncensored Data and of Singly Right-censored Data Utilizing the Persson and Rootzen Method.*

JEDEC JESD61, *Isothermal Electromigration Test Procedure.*

JEDEC JESD63, *Standard Method for Calculating the Electromigration Model Parameters for Current Density and Temperature.*

JEDEC JESD87, *Standard Test Structures for Reliability Assessment of AlCu Metallization with Barrier Materials.*

JEDEC JEP139, *Guide for Isothermal Aging Method to Characterize Aluminum Interconnect Metallization for Stress-Induced Voiding.*

JEDEC JEP 159, *Procedure for the Evaluation of Low-k/Metal Inter/Intra-Level Dielectric Integrity*

6.1.3 Endurance tests

JEDEC JESD22-A104, *Temperature Cycling.*

JEDEC JESD22-A113, *Preconditioning of Surface Mount Devices prior to Reliability Testing.*

JEDEC JESD47, *Stress-Test Driven Qualification of Integrated Circuits.*

JEDEC JESD50, *Special Requirements for Maverick Product Elimination.*

JEDEC JESD85, *Methods for Calculating Failure Rates in Units of FITs.*

6.2 Selected references

Meeker, Q.A. and L.A. Escobar, *Statistical Methods for Reliability Data,* John Wiley, 1998.

Tobias, P.A. and D.C. Trindade, *Applied Reliability,* 2nd Ed., CRC Press, 1995.

Nelson, Wayne, "Accelerated Testing: Statistical Models, Test Plans, and Data Analyses", in *Wiley Series in Probability and Mathematical Statistics-Applied Probability,* John Wiley, 1990.

Amerasekera, E.A. and F.N. Najm, *Failure Mechanisms in Semiconductor Devices,* 2nd Ed., John Wiley, 1997.

Ohring, Milton, *Reliability and Failure of Electronic Materials and Devices,* Academic Press, 1998.

Yue, John, "Reliability", in C.Y. Chang and S.M. Sze (eds.), *ULSI Technology,* McGraw-Hill, 1996, Chapter 12.

Takeda, E. et al, *Hot-Carrier Effects in MOS Device,* Academic Press, 1995.

Amerasekera, E.A. and Charvaka Duvvury, *ESD in Silicon Integrated Circuits,* John Wiley, 1996.

IRPS Conference Proceedings and Tutorials are an excellent source of information on current test methodologies and reliability models. (Web site www.irps.org)

Microelectronics Reliability, Pergamon Press. This journal publishes the proceedings of ESREF, the European equivalent of IRPS, along with frequent review papers.

Abadeer, W.W., IEEE Transactions on Device and Materials Reliability, Vol. 1, No. 1, March 2001, *Reliability Monitoring and Screening Issues With Ultrathin Gate Dielectric Devices.*

7 Qualification test summary table

Section	Procedure	JEDEC Reference Standard(s)	Other Standards	Qual or Eng
8.1	Electromigration	JESD61, JESD87, JESD33A, JESD37, JESD63, JEP122G	ASTM: F1260-96 EIAJ-986	Q
8.2	Stress Migration (Stress-Induced Voiding)	JEP139, JESD87, JEP122		Q
8.3	Thermal Cycling (Copper Interconnect)	JESD22-A104		Q or E
8.4	Inter/Intra Metal-Dielectric Reliability	JEP159		Q
8.5	Yield Data & Defect Density Calculation	None		Q

8 BEOL Interconnect Reliability

8.1 Electromigration

Electromigration testing should be done on each unique via level and metal layer (i.e., having any differences in design rules or process parameters from the rest of the metal stack, including the metal and inter-/intra- level dielectric processes. For instance, if metal layers and vias 2-4 have the same design rules and undergo similar processing, testing of metal 2 and connecting vias (lowest similar metal level) will suffice. The worst-case stacked via structure (if known), or each permutation of stacked vias, should be tested separately. Via tests should exercise electron flow both up and down through the via, thus stressing both via-to-metal interfaces.

The method described in this section may have limitations when applied to newer technologies (e.g., Cu/Low K). In such instances, the applicability of the method should be evaluated on a case-by-case basis.

8.1.1 Electromigration test requirements

Reference procedure	ASTM F1260-96, *Standard Test Method for Estimating Electromigration Median Time-To-Failure and Sigma of Integrated Circuit Metallization.* JEDEC JESD33-A, *Standard Method for Measuring and Using the Temperature Coefficient of Resistance to Determine the Temperature of a Metallization Line.* JEDEC JESD37, *Standard Lognormal Analysis of Uncensored Data and of Singly Right-censored Data Utilizing the Persson and Rootzen Method.* JEDEC JESD63, *Standard Method for Calculating the Electromigration Model Parameters for Current Density and Temperature.* JEDEC JESD87, *Standard Test Structures For Reliability Assessment of Al-Cu Metallization With Barrier Materials.*
Test structures	Test structures for Al metallization are recommended to be designed for each combination of line and via/contact, per JEDEC JESD87, *Standard Test Structures For Reliability Assessment of AlCu Metallization With Barrier Materials*. Test structures for Cu can be designed according to JESD87. Structures should be included that allow measuring the influence of current flow direction and reservoir and back-stress effects. However, for Cu metallization with no barrier layer on the top surface, additional structures should be included that have a line width sufficiently larger than the width of the via (e.g., 2-5X) above to prevent contact between the via above and the liner of the test line.
Vehicle	Test structures may be stressed at package or wafer level. For package level tests, ceramic packages should be used.
Sample size and stress conditions	a) In a standard process qualification, samples from at least 2 lots with 2 wafers per lot should be tested for every structure referenced under “Test Structures” above. At least a third lot should be tested if substantial variations are observed between the first two lots. b) Samples from 1 lot are to be used for determination of Black’s equation parameters. A minimum of three current densities ($J_1<J_2<J_3$) and three temperatures ($T_1<T_2<T_3$) are recommended. Current density and temperature values should be within the limits outlined under “Test Method” below. - To determine the activation energy, stress a minimum of three groups at J_2/T_1, J_2/T_2, and J_2/T_3. - To determine the current density exponent, stress a minimum of two additional groups at J_1/T_2 and J_3/T_2, using the J_2/T_2 group from the temperature stresses to complete the current group. c) Sample Size Considerations i) A minimum starting sample size of 15 per experiment (for each test structure for each unique set of test conditions) is required to provide accurate estimation of t_{50} and σ, and a minimum sample size of 20 is recommended. ii) A minimum of 12 valid time-to-fail data points is required (for each test structure for each unique set of test conditions) for determination of t_{50} and σ If there are less than 12 valid time-to-fail data points for an individual experiment, that experiment must be repeated. iii) No more than 50% of the sample data can be censored, i.e., at least 50% of the samples must be taken to failure. iv) In a multi-cell test, the 50% failure requirement may be waived for the cell with the lowest acceleration, provided the data for all cells can be fit with a common sigma.

8.1.1 Electromigration test requirements (cont'd)

Test parameters & Failure Criteria	a) Test parameters include stress temperature (*Ts*), stress current density (*Js*) and percent resistance change when the sample fails. Percent resistance change is defined as: $[(R_{INITIAL}-R_{FINAL})/R_{INITIAL}] \times 100$, where $R_{INITIAL}$ is the initial resistance and R_{FINAL} is the final resistance measured at the stress temperature. b) Failure criteria: either a percent resistance change or a leakage limit to an extrusion monitor. The appropriate failure limit (e.g., 2%, 5%, 10% or 20% resistance change, or Amps of leakage current) will depend on the functionality specification for the technology.
Test Method Cautionary Note	a) After determining the temperature coefficient of resistance (TCR) and measuring $R_{INITIAL}$, parts should be subjected to constant-current stressing at 150 °C – 300 °C for Al, and at 250 °C – 400 ° C for Cu, in conventional ovens and at current densities ranging from the target J_{MAX} up to five times J_{MAX}, until sufficient parts have failed (see c) and d) in "Sample size and stress conditions" above). R_{FINAL} and the failure time must be recorded for each part that fails. Test structure temperature must be determined from the TCR according to JESD33, and the corrected temperature (oven ambient plus Joule heating) should be used for calculations in b) below. Performing the test at higher temperatures may be suitable in certain cases (e.g., for Cu metallization with a metal cap). b) The test plan should allow for extraction of the activation energy (*Ea*) and the current density exponent (*n*) for the Black's equation model, consistent with JESD63. c) Consistent with ASTM F1260-96, the resistance increase of the test structure and leakage to the extrusion monitor shall be measured within periods that are much shorter than the anticipated duration of the test. Each experiment in the test plan should be continued at least until the number of failures reaches the larger of the following conditions: 1) at least 50% of the samples have failed, or 2) at least 12 samples have failed when the experiment sample size is < or = 24. d) Failure analysis of representative failure samples is recommended. (If No Failure analysis is performed, data analysis based on % cumulative failure may be misleading when different fail mechanisms are present) The methodology outlined above allows for the derivation of an EM model for the metallization being tested. If the suggested sample requirements and/or the minimum number of allowed failures cannot be produced within a reasonable time, it may not be possible to derive such a model. However, it may be possible to establish a lower bound on lifetime for a given set of stated conditions, and demonstrate that qualification goals are met.
Model to be used	a) The models are described in JEP122G 1. For Al interconnects see section 5.9 2. For Cu interconnects see section 5.10

8.1.1 Electromigration test requirements (cont'd)

Merit data

Calculate either 1) or 2) below, using the parameters in the table.

1) Lifetime for a 0.1% fraction failure per structure at the intended maximum current density and intended maximum operating temperature for the technology, using the following formula.

$$\tau(0.001) = t_{50_{stress}} \bullet \left(\frac{J_{stress}}{J_{use}}\right)^{n} \exp\left[-3.09\sigma + \frac{Ea}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{stress}}\right)\right]$$

2) Maximum current density (J_{MAX} 0.1%) for a per-structure failure fraction of 0.1%, at the intended maximum operating junction temperature and the maximum intended lifetime using the following formula.

$$J_{MAX}(0.001) = J_{stress} \bullet \left\{\frac{\left[t_{50stress} \bullet \exp\left(-3.09\sigma + \frac{E_a}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{stress}}\right)\right)\right]}{\tau}\right\}^{\left(\frac{1}{n}\right)}$$

Parameter	Description	Units
T_{use}	Maximum operating junction temperature plus applicable Joule heating	K
τ	Maximum power-on lifetime	hr
J_{stress}	Current density during stress	mA/μm^2
T_{stress}	Temperature during stress, including Joule heating	K
σ	Lognormal sigma of the failure distribution	
$t_{50stress}$	Lognormal median time to failure from the failure data	hr
E_A	Activation energy from failure data, as indicated above	eV
n	Current density exponent from failure data	
k	Boltzmann Constant = 8.6174 x 10^{-5}	eV/ K

Note: In formula (1) and (2), the coefficient of σ, -3.09, is the random variable in the Standard Normal Distribution corresponding to 0.1% cumulative fraction (summed from the left side) of the population of each structure being tested. It is only one example to show how to perform these calculations. In reality, chip level failure rate related to EM is a statistical sum of all different structures and their instances in a chip. Therefore, other coefficient values may be considered for specific application requirements and design constraints, and can be chosen case by case or per customer and supplier arrangements. The calculated lifetime, maximum use current density, and chip level failure rate related to EM will be different for other coefficient values.

Other data required

a) Line width, thickness, sheet resistance and composition of metal lines, via dimensions and measurements of alignment of via/contact layers to their respective metal layers.

b) In the event that failure distributions are bi-modal, or if early failures occur, failure analysis should be provided to compare the failures of the different distributions.

8.1.2 Reporting requirements

The final report should include the following details as general guidelines. Detailed reporting should conform to any pre-existing agreements between the customer and the supplier.

1) Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2) Back-end scheme: thickness, composition for each layer, via type (Tungsten, etc.), inter-level dielectric, capping layers, etch-stop layers.
3) Relevant design rules: minimum widths, minimum spacing, contact and via sizes, minimum overlaps of metal to contact and via,
4) Relevant description of test structures (metal level, line width & length, number and placement of contacts or vias, etc.).
5) For each experiment in the experimental plan:
   a) Test conditions (Nominal T_{STRESS}, Actual T_{STRESS}, J_{STRESS}), room temperature and stress temperature resistances.
   b) Starting Sample size, raw failure data, failure criteria, lognormal plot of failure time data, percent valid fails at end of test.
   c) Sample estimates (nominal values) of $\mathbf{t_{50}}$ and sigma with their 90% confidence limits, and the method used to determine sample estimates and confidence intervals.
6) Extracted Black's equation parameters: activation energy (E_A), current density exponent (n) consistent with JESD63 using Black's model. Construct a 90% confidence interval about the best fit projected lifetime at the maximum operating temperature and maximum current density.

8.2 Stress migration (stress-induced voiding)

Testing should be done on all metal layers which differ from previous technologies in dimensions, passivation or metallization and interconnections (vias, studs, etc.). For technologies which use the same processes for multiple layers, the focus should be the layers with the smallest ground rules and the thickest total passivation layer (typically M1).

NOTE the methodology outlined below allows for the modeling of stress voiding for the metallization process. If the methodology is not adhered to, or if it was not possible to collect adequate failure statistics, it may not be possible to extract a degradation model.

8.2.1 Stress migration/ stress-induced voiding requirements for Aluminum interconnect (*may serve as reference ONLY for Cu interconnect)*

Reference procedure	JEP139, *Guide for Constant Temperature Aging to Characterize Aluminum Interconnect Metallization for Stress-Induced Voiding.* JEDEC JESD37, *Standard Lognormal Analysis of Uncensored Data, and of Singly Right-censored Data Utilizing the Persson and Rootzen Method.* JEDEC JESD87, *Standard Test Structures For Reliability Assessment of AlCu Metallization With Barrier Materials.*
Test parameters	Relative resistance change per JEP139.
Test structures	1) Metal lines: Kelvin-connected serpentines & mazes with min line width, and lengths >=5,000µm 2) Via chains: Short-line and long-line chains of which the metal lines should be >=5,000µm
Vehicle	Wafer Level or package level
Method	For Al interconnects per JEP139, For a completely new metallization: 1) Select multiple (≥3) wafers from each of multiple (≥3) wafer lots 2) Measure sheet resistances and line resistances of relevant structures 3) Separate wafers into multiple groups: 1 to 2 wafers per lot in each group 4) Age the multiple wafer groups at multiple temperatures (e.g., 175, 200, 225, 250 & 275 °C) 5) Take readouts of resistance measurements at selected intervals (e.g., 24, 48, 100, 250, 500, 750, 1000 & 2000 hours) 6) Per JEP139, failure criterion is a percent increase in resistance, dependent on the functionality requirements of the technology. 7) Plot the failure times on a lognormal probability plot (per JESD37) to determine sample estimates of $\mathbf{t_{50}}$ and sigma and to check log-normality of the data. 8) Determine effective activation energy, Δh (per JEP139) 9) Determine acceleration factor, AF (JEP139 equation 3) NOTE An abbreviated version of this procedure is acceptable for well-understood processes, and would permit using just one wafer per lot and three temperatures, which would embrace the temperature of peak voiding. OPTIONAL To further understand the impact of stress-induced voids on the metal interconnects, a wafer level or package level electromigration test can be performed on the aged samples, as well as unstressed samples from the same lot.
Model to be used	For Al interconnects see JEP122 section 5.12
Sample size	Min 120 per temperature, per metal level, or as appropriate to obtain a statistically valid sample and provide spatial information. Consider selecting samples from multiple wafers and lots as listed above.
Merit number	Application dependent merit number are to be determined by the foundry and the customer (*for example: no fail per structure for 1000hr stress at various temperatures with sample size ≥ 50*)
Other data required	Test structure characteristics: width, height, length, resistance, and relative alignment of metal to via.

8.2.2 Report requirements

These guidelines should not replace any existing agreements between customers and suppliers regarding specific information for reporting purposes.

1) Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2) Back end scheme: thickness, composition for each layer, via type (Tungsten, etc.), inter-level dielectric, passivation deposition temperature.
3) Relevant design rules: minimum widths, minimum spaces, contact and via sizes.
4) Brief description of test structures and test conditions (T_{STRESS})
5) Sample size, lognormal plot of failure time data, percent fails at end of test, lognormal $\mathbf{t_{50}}$ and sigma.
6) Extracted parameters for stress migration model: activation energy, pre-exponent.
7) Projected lifetime for the target failure rate (e.g. 0.1%, 1ppm, etc.) @ maximum operating temperature.

8.3 Thermal cycling

A thermal cycling measurement is required during qualification to assure the robustness of Cu/SiO2 and/or Cu/low-k stacks in terms of voiding or delamination of the copper interconnects. It is also applicable for the qualification of Aluminium interconnects. Testing should be done on all metal layers which differ from previous technologies in dimensions, passivation or metallization and interconnections (vias, studs, etc.) For technologies that use the same processes for multiple layers, the focus should be on the layers with the smallest ground rules and the thickest total passivation layer (typically M1).

8.3.1 Thermal cycling test requirements

Reference procedure	No JEDEC standard available. However, stress conditions should be equivalent to those applied to the pilot product (TQV) at package level, per JESD22-A104. JESD87, *Standard Test Structures For Reliability Assessment of AlCu Metallization With Barrier Materials.*
Test parameters	The resistance shift of the interconnect structure is recorded during thermal cycling.
Test structures	The same test structures as for stress migration measurements can be used: a) Metal layer x and metal layer x+1 with a single via/contact (or a sea of vias). Using the design rules, the geometry of one metal layer is a wide line, e.g., large area of metal, while the geometry for the other is min (narrow line). All permutations should be covered, especially when metal layer material (from Cu to Al) or IMD changes (e.g., from low-k to SiO2) from one metal level to the next. b) Stacked via/contact structures of all permutations should be tested especially with maximum and minimum geometries allowed by the design rules. c) Via/contact chains with minimum via/contact geometries and minimum spacing between vias/contacts and minimum line widths. Lines can form any type of serpentines or mazes.
Vehicle	Wafer level stress in oven, or self-heated.
Method	Do one of the following: a) 500 cycles from -65 °C - +150 °C, or b) 1000 cycles from -55 °C to +125 °C, or c) An equivalent temperature range may be used with different upper and lower temperature limits but the same ΔT (e.g., +30 °C to +210 °C). d) Alternative cycling scheme and range with technical justification. NOTE 1 For cases (a) or (b) above, the temperature ramp rate and soak conditions are as specified in 22-A104. NOTE 2 Alternate scheme may include the use of a heated wafer chuck, or possibly a self-heated structure.
Model to be used	None available. In the absence of a proven model, only field product evaluations would prove conclusively the reliability of the process.
Sample size	Minimum: 120 (all die on the wafer * 1 wafer * 3 lots) per temperature for all permutations of the test structures or as appropriate to obtain statistically valid samples and provide spatial information. The measured devices should be uniformly spaced across the wafer for wafer mapping purposes.
Merit number	A significant resistance increase (e.g., > 5%, 20%, 100%) indicates severe stress voiding or delamination. The failure criterion should be chosen according to the robustness of the product.
Other data required	Lot identification; wafer number; die location; details of interconnect and via/contact geometry: width, height, length, resistance before stress, relative alignment of via/contact to metal line.

8.3.2 Report requirements

These guidelines should not replace any existing agreements between customers and suppliers regarding specific information for reporting purposes.

1. Fab name and location; process name, lot number, wafer number and date code, and certification that material tested represents wafers of current process qualification.
2. Back end scheme: thickness & composition of each layer and via/contact type (tungsten etc.), inter-level dielectric, passivation deposition temperature.
3. Relevant design rules: min. widths, min. spaces, min. via/contact sizes.
4. Brief description of test conditions.
5. Sample size per lot for each measurement, plot of resistance change, percentage of fails at the end of the stress, lognormal t50% and sigma.
6. When problems occurs deliver relevant failure analysis investigations on all affected wafers for the clear identification of the root cause.

8.4 Inter/intra-metal dielectric integrity

This test may be done during qualification, or as part of an engineering study. The insulation characteristic of an inter/intra-metal dielectric layer (IMD) is required to be studied. The dielectric between metal lines of one metal layer is defined as intra-metal dielectric, and the dielectric between metal lines of two conjunctive metal layers is defined as inter-metal dielectric. In general, both intra-metal dielectric and inter-metal dielectric should be tested. Testing should be performed on all IMD layers especially when the metal layer scheme changes. Due to the unique nature of ILD Cu/low-k dielectric system, it is essential that the dielectric failure criteria should be carefully specified.

8.4.1 IMD test requirements

Reference procedure	JEP159 - *Procedure for the Evaluation of Low-k/Metal Inter/Intra-Level Dielectric Integrity*
Test parameters	a) Leakage current through the IMD at maximum operating voltage (V_{DDMAX}) before the reliability stress. b) For the ramped voltage stress test: ▪ Weibull distribution of the voltage to failure (V_{FAIL}). ▪ Record the complete extrinsic and intrinsic branches of the distribution. c) For the constant voltage stress: ▪ Weibull distribution of the time to failure (t_{FAIL}). ▪ Normal distribution of the leakage current @ V_{DDMAX} before and after stress.
Failure criteria	a) For the ramped voltage stress test: Failure is defined by the leakage current exceeding a specified value at the stress temperature, e.g., equal to the IMD leakage current specification or by 2) a sudden leakage drop at the stress temperature indicating an open circuit failure caused by the breakdown current surge destroying a segment of the interconnect metallization. b) For the constant voltage stress: Failure is defined 1) by the leakage current exceeding a specified value at the stress voltage and temperature. This value may be calibrated relative to the IMD leakage current specification at V_{DDMAX} or by 2) a sudden leakage drop at the stress temperature indicating an open circuit failure caused by the breakdown current surge destroying a segment of the interconnect metallization.

8.4.1 IMD test requirements (cont'd)

Test structures	a) For modelling, three different sizes (dielectric area between metal lines) should be tested. Once the model has been verified, one size is sufficient for qualification. b) Line only structures and Via related structures are recommended for testing line level TDDB and Via TDDB: ▪ A metal serpentine with two metal combs inserted from each side to cover both edges of the serpentine (range of lengths e.g., 10mm, 10cm, 3m) or two metal combs inserted in each other (no serpentine) covering various critical constellations of ILD layers . ▪ Via related structures such as two via chains interwoven (# of vias in chain e.g., 1E3, 1E5, 1E7) covering various critical constellations of ILD layers. ▪ Stacked line level structures can be used for inter-level test ▪ Minimum spacing between metal lines to be used. Additionally, when high voltage applications are required, a wider spacing must be also tested.
Vehicle	Wafer level or package level measurements.
Method	Stress to be done at the worst case chip operating temperature (e.g., +125 °C or greater): 1. Ramped voltage stress to failure, or 2. Constant voltage stress at ~ $2V_{DDMAX}$ OR PROBABLY GREATER (the optimal value of V_{STRESS} to be determined experimentally). Stress should continue until 50% or more of the samples exceed the failure criterion.
Model to be used	JEP159 and Reference to recent published papers at IRPS (2005-2013)
Sample size	a) For the largest structure size and for all various constellations of IMD layers: Minimum 120 (20 Die * 2 wafers * 3 lots). b) For the other two structure sizes: A minimum of 40 (20 Die * 2 wafers *1 lot) is required for all various combinations of IMD layers. The measured devices should be uniformly spaced across the wafer for wafer mapping purposes. Either wafer or packaged test structures may be used for testing.
Merit number	1. The leakage current at operating voltage (V_{DDMAX}) before stress. 2. For the ramped voltage test: Defect density may be determined by using the general formula below (see JESD35-A) $C \le 1 - \sum_{i=Y}^{N} \frac{N!}{i!(N-i)!} \left[\exp(-D_o A_t)\right]^i \left[1 - \exp(-D_o A_t)\right]^{N-i}$ Where Y is the minimum acceptable number of non-defective IMD devices found among the N IMD devices tested, C is the confidence level, D_0 is the acceptable defect density, A_t is the effective area of each test structure, N is number of test structure sampled. The data analysis begins by plotting the cumulative breakdown distribution versus Ebd on Weibull scale. If such a plot results in a bimodal or other multi-modal distribution, a separation point between extrinsic and intrinsic distribution could be identified, and then the defective fraction, F=(1-Y)/N, also can be determined. ▪ It is recommended to assess the area scaling of the V_{FAIL} results between the three differently sized test structures against the Poisson Model. If a strong die-to-die variation exists across a wafer, Poisson area scaling model could be broken and gives a pessimistic scaling result for compound Weibull distributions. 3. For the constant voltage stress: ▪ No merit number is defined. However, it is possible to derive a lifetime model following a methodology analogous to that outlined for TDDB testing. 4. For TDDB area scaling, it is recommended to assess the area scaling of the t_{FAIL} results between the three differently sized test structures against the Poisson Model. If Poisson area scaling model can't be applied on experimental data, usually due to compound Weibull distributions caused by die-to-die variations, using TDDB data from the largest available test structure is recommended for lifetime projection unless a new area scaling model is derived.
Other data required	Lot identification; wafer number; die location; thickness of IMD; details of serpentine/comb geometry: width, height, length, spacing.

8.4.2 Report requirements

These guidelines should not replace any existing agreements between customers and suppliers regarding specific information for reporting purposes.

1. Fab name and location; process name, lot number, wafer number and date code, and certification that material tested represents wafers of current process qualification.
2. Back end scheme: thickness & composition of each inter-level dielectric and metal layer and passivation deposition temperature.
3. Detailed description of test conditions: stress time, step time, stress bias, voltage increment, breakdown criteria, and min/start and max/stop voltage.
4. Sample size per lot for each measurement; representative plots of leakage current; percentage of initial leakage fails; Weibull distribution of V_{FAIL} data; Defect density at intersection extrinsic/intrinsic branches and V_{FAIL} at 63.2%.
5. Raw data should be supplied to the customer upon request.

8.5 Detailed yield results

Reference procedure	None
Test parameters	Full Functional Test and I_{DDQ} and Leakage Tests
Test structures	Appropriate technology qualification vehicle
Vehicle	Wafer Probe
Method	NA
Model to be used	Foundry Will specify Yield Model
Sample size	12 wafers from each of 6 lots
Defect density	Defects per square centimeter
Other data required	1) Area of SRAM or other qualification vehicle 2) # of Critical Layers Used 3) Site location information relative to edge exclusion zone

8.6 Report requirements

These guidelines should not replace any existing agreements between customers and suppliers regarding specific information for reporting purposes.

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Brief description of technology qualification vehicle: chip area, GOX area, circuit type (e.g., SRAM, ASIC), etc.
3. Test methodology & Test coverage, test speed (frequency), I_{DDQ} limits.
4. Number of devices tested, devices passed and percent yield for each wafer tested.
5. Defect density per square cm.

- Metal integrity
  - Non-planar technologies: Isolation & Continuity Metal1/Metal2/Metal3 over topologies for filament (also known as short, ribbon, stringer).
  -
- EM
  - Short high temperature isothermal stress or similar test.

4. Resistors (Implant or thin film resistors))
   - Contact resistance
   - Sheet resistances (If different than other measured sheet resistances)
   - Width reduction, calculated from resistance measurements on two resistors with different widths
   - Resistor values
   - Resistances for specific widths already measured for width calculations
   - Maximum current ratings
   - Self-heating and aging effects

9 Construction analysis

9.1 Construction analysis

Construction analysis is an essential tool to aid in evaluating process limitations and interpreting yield and reliability data. Construction analysis data provided by the foundry as part of the qualification package allows the customer to better understand the dependencies of their product on specific design rules. This may not substitute for detailed construction analysis done by the customer on the customer's own product.

Constructional analysis shall be performed on wafer or die to check the quality features. Any anomaly which has been encountered during the constructional analysis shall be documented and communicated to the appropriate engineering group for corrective action. Additional work shall be supplemented as required by the process technology.

The constructional analysis results (visual or measurements) shall be documented in detail to demonstrate process attributes distribution. All visual documentation (Optical or SEM photos) shall display best case, typical, and worst case features. The parametric measurements shall record low, average, high and sigma values.

9.1.1 Construction analysis requirements

Reference procedure	None
Test parameters	A DUT is considered to fail if the design rule and physical measurement do not match in size shape or function.
Test structures	a) Topographical SEM photos of minimum Metal, poly b) Cross sectional SEM photos of all critical levels including each metal level, via, contact, poly, oxides and silicon isolation scheme.
Vehicle	Fully processed baseline wafers.
Method	a) Optical photographs for wide angle views and orientation location b) SEM of each individual layer and c) TEM of gate oxide and flash oxides.
Model to be used	
Sample size	Three lots with a minimum one die.
Merit number	The variation in film thickness and/or line-width should be consistent with design manual assumptions.
Other data required	Line width, thickness, composition of metal lines, via dimensions and alignment to metal lines.

9.1.2 Reporting requirements

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Back end scheme: thickness, composition for each layer, via type (Tungsten, etc.), inter-level dielectric. Relevant design rules: minimum widths, minimum spaces, contact and via sizes.

Annex A (informative) Differences between revisions

A.1 Differences between JEP001-1A and JEP001A

The following list briefly describes most of the changes made to entries that appear in this publication, JEP001-1A, compared to its predecessor, JEP001A (February 2014).

Clause	Description of Change
All	JEP001A Split into three parts: JEP001-1A Backend of Line, JEP001-2A, FEOL END Transistor Level and JEP001-3A Product level.

Standard Improvement Form JEDEC JEP001-1A

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

_____

3. Other suggestions for document improvement:

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